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REMARKS

Claims 1-25 are cancelled without prejudice to their underlying subject matter. Applicant amends claims 26-28 and 33-40. Attached hereto is a marked-up version of the changes made to the claims by the current amendment.

Claims 26-32 and 37-40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent number 5,313,101 (Harada et al.) in view of U.S. patent number 5,281,850 (Kanamori). Applicant respectfully traverses this rejection.

Claim 26, as amended, defines a semiconductor device and recites, in part, "a titanium aluminide layer lining at least a bottom of the via hole" and "a conductive material on the titanium aluminide layer, said conductive material and said titanium aluminide layer being in contact at an interface, said interface being substantially free from tensile stress between said titanium aluminide layer and said conductive material." The combination of Harada et al. and Kanamori does not teach or suggest such a device.

As has been noted in previous responses to office actions during this prosecution, Harada et al. discloses that its titanium aluminide layer is formed by: (1) depositing a titanium film (101) in a via hole (see column 9, specifically lines 41-46) over an aluminum layer (4); (2) depositing a titanium nitride film (102) over the titanium film (see column 9, lines 49-51); (3) depositing an uppermost second aluminum interconnection layer (100) over the titanium nitride film (102) (see column 10, lines 19-23); and (4) heat treating *after* depositing layer (100) for about 15-60 minutes at a temperature of 300°-450° C so that the compound $TiAl_3$ is formed at the bottom of the via by the heat treatment (column 10, lines 29-39). Since Harada et al.'s heat treatment is initiated *after* all the layers (*i.e.*, the titanium layer, the titanium nitride layer, and the top aluminum layer) have been deposited over the aluminum layer (4), upon becoming titanium aluminide, the bottom layer (which is in intimate contact with the overlying layers) inherently and necessarily densifies and contracts, exerting tensile stress upon the overlying titanium nitride layer and

potentially creating undesirable voids and cracks in this layer. Thus, Harada et al. does not teach or suggest the invention of claim 26.

In considering any patent as a reference for 35 U.S.C. § 103 purposes, it must be considered as a whole, including any teaching away, and further, it must suggest the desirability and obviousness of combining it with the other references. M.P.E.P. §§ 2141.01 and 2141.02 (2001) (emphasis added). In accordance with M.P.E.P. § 2144.05.III, a prima facie case of obviousness is rebutted by showing that a reference, in any material respect, teaches away from the claimed invention. M.P.E.P. § 2144.05.III (2001) (emphasis added), citing In re Geisler, 116 F.3d 1465, 1471, 43 U.S.P.Q.2d 1362, 1366 (Fed. Cir. 1997). "A prior art reference that 'teaches away' from the claimed invention is a significant factor to be considered in determining obvious." M.P.E.P. § 2145.X.*D*.1 (2001). "References cannot be combined where [a] reference teaches away from their combination" for the purposes of supporting a rejection under 35 U.S.C. § 103(a). Id. at X.*D*.2.

As described above, Harada et al. is actually teaching away from the claimed subject matter. As a teaching away reference, Harada et al. is not properly combined with Kanamori or any other reference for the purposes of rejecting the claims under 35 U.S.C. § 103(a).

The Kanamori description cannot overcome the deficiencies of the Harada et al. reference. There is no teaching or suggestion anywhere in Kanamori that a titanium aluminide layer is in contact with an overlying layer and does not exert tensile stress upon that overlying layer. In fact, combining Kanamori and Harada et al. is improper because, as noted above, Harada et al. teaches away from the claimed invention and combination of references. Thus, the subject matter of claim 26 would not have been obvious over Harada et al. in view of Kanamori.

Claim 27, as amended, defines a semiconductor device and recites, in part, "a titanium aluminide layer lining at least a bottom of the via hole" and "a titanium nitride layer substantially free of through cracks on the titanium aluminide layer, wherein said titanium nitride layer is in contact with said titanium aluminide layer at an interface that is substantially free of tensile stress between said titanium aluminide layer and said titanium nitride layer." As discussed above regarding the patentability of claim 26, the combination of Harada et al. and Kanamori does not teach or suggest at least the above recited portion of the claim. Further, also as noted above, Harada et al. teaches away from the recited interface being substantially free of tensile stress, making its combination with other references for a rejection under 35 U.S.C. § 103(a) improper. Thus, the subject matter of claim 27 would not have been obvious over Harada et al. in view of Kanamori.

Claim 28, as amended, defines a semiconductor memory device and recites, in part, "a titanium aluminide layer lining at least a bottom of the via hole" and "a titanium compound layer on the titanium aluminide layer and in contact with said titanium aluminide layer at an interface that is substantially free of tensile stress." As discussed above, Harada et al. does not teach or suggest that the interface recited is substantially free of tensile stress, and in fact, teaches away from this. For at least the same or similar reasoning as set forth above regarding the patentability of claims 26 and 27, the subject matter of claim 28 is patentable over Harada et al. and Kanamori, taken individually or in combination. Further, claims 29-32 depend from claim 28 and are likewise patentable over Harada et al. and Kanamori, alone or in combination.

Claim 37, as amended, defines a computer system having a random access memory and recites, in part, "a titanium aluminide layer lining at least a bottom of the via hole" and "a titanium compound layer on the titanium aluminide layer, wherein said titanium compound layer is in contact with said titanium aluminide layer at an interface, said interface being substantially free of tensile stress between said titanium aluminide layer and said titanium compound layer." As discussed above, Harada et al. does not teach or

suggest that the recited interface is substantially free of tensile stress, and in fact, teaches away from this. For at least the same or similar reasoning as set forth above regarding the patentability of claims 26-28, the subject matter of claim 37 is patentable over the combination of Harada et al. and Kanamori.

Claim 38, as amended, defines a computer system having a random access memory and recites, in part, "a preformed titanium aluminide layer lining at least a bottom of the via hole" and "a conductive material on the titanium aluminide liner, wherein said conductive material is in contact with said titanium aluminide layer at an interface, said interface being substantially free of tensile stress between said titanium aluminide layer and said conductive material." As discussed above, Harada et al. does not teach or suggest that the recited interface is substantially free of tensile stress, and in fact, teaches away from this. For at least the same or similar reasoning as set forth above regarding the patentability of claim 26, the subject matter of claim 38 is patentable over the combination of Harada et al. and Kanamori.

Claim 39, as amended, defines a computer system having a random access memory and recites, in part, "a titanium aluminide layer lining at least a bottom of the via hole" and "a titanium nitride layer substantially free of through cracks on the titanium aluminide layer, wherein said titanium nitride layer is in contact with said titanium aluminide layer and said titanium aluminide layer exerts approximately zero tensile stress upon said titanium nitride layer." As discussed above, Harada et al. does not teach or suggest that the recited underlying titanium aluminide layer does not exert tensile stress upon the overlying titanium nitride layer recited, and in fact, teaches away from this. For at least the same or similar reasoning as set forth above regarding the patentability of claim 26, the subject matter of claim 39 is patentable over the combination of Harada et al. and Kanamori.

Claim 40, as amended defines a computer system having a random access memory and recites, in part, "a titanium aluminide layer lining at least a bottom of the via

hole" and "a titanium compound layer on the titanium aluminide layer, wherein said titanium compound layer is in contact with said titanium aluminide layer at an interface, said interface being substantially free of tensile stress between said titanium aluminide layer and said titanium compound layer." As discussed above, Harada et al. does not teach or suggest that the recited interface is substantially free of tensile stress, and in fact, teaches away from this. For at least the same or similar reasoning as set forth above regarding the patentability of claim 26, the subject matter of claim 38 is patentable over the combination of Harada et al. and Kanamori.

Because the combination of Harada et al. and Kanamori is improper, and even if, assuming arguendo, such combination was proper, it does not teach or suggest the subject matter claimed, claims 26-28 and 37-40 are patentable over Harada et al. and Kanamori, taken alone or in combination. Applicant respectfully request that the 35 U.S.C. § 103(a) rejection of claims 26-32 and 37-40 be withdrawn.

Claims 33-36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Harada et al. in view of Kanamori (as applied to claim 28) and further in view of U.S. patent number 4,656,605 (Clayton). Applicant respectfully traverses this rejection.

Claim 33, as amended, defines a memory module having a random access memory and recites, in part, "a titanium aluminide layer lining at least a bottom of the via hole" and "a titanium compound layer on the titanium aluminide layer, said titanium compound layer being in contact with said titanium aluminide layer, wherein said titanium compound layer experiences approximately no tensile stress from said titanium aluminide layer." As with claims 26-32 and 37-40, discussed above as patentable over Harada et al. and Kanamori, such combination of references does not teach or suggest (and in fact teaches away from) that a titanium compound layer overlying a titanium aluminide layer experiences approximately no tensile stress from the titanium aluminide layer, as claimed. Additionally, Clayton can add no teaching or suggestion to supplement Harada et al. and Kanamori to overcome their instructional deficiencies. The subject matter of claim 33

would not have been obvious over Harada et al., Kanamori, and Clayton, alone or in combination.

Claim 34, as amended, defines a memory module having a random access memory and recites, in part, "a titanium aluminide layer lining at least a bottom of the via hole" and "a conductive material on the titanium aluminide layer, wherein said conductive material and said titanium aluminide layer are in contact at an interface having approximately no tensile stress from said titanium aluminide layer." As discussed above regarding the patentability of claim 33, Clayton does not offer any teaching or suggestion to overcome the lack of teaching or suggestion by Harada et al. and Kanamori of the recited interface having approximately no tensile stress from the titanium aluminide layer. Thus, Harada et al., Kanamori, and Clayton, alone or in combination, would not have rendered the subject matter of claim 34 obvious.

Claim 35, as amended, defines a memory module having a random access memory and recites, in part, "a titanium aluminide layer lining at least a bottom of the via hole" and "a titanium nitride layer substantially free of through cracks on the titanium aluminide layer, wherein said titanium nitride layer is in contact with said titanium aluminide layer at an interface, said interface being substantially free of tensile stress between said titanium aluminide layer and said titanium nitride layer." For at least the same reasoning set forth above for the patentability of claims 33 and 34, claim 35 would not have been obvious over Harada et al., Kanamori, and Clayton, alone or in combination.

Claim 36, as amended, defines a memory module having a random access memory and recites, in part, "a titanium aluminide layer lining at least a bottom of the via hole" and "a titanium compound layer on the titanium aluminide layer at a contact interface, wherein said contact interface experiences approximately no tensile stress from said titanium aluminide layer." For at least the same reasoning set forth above regarding the patentability of claims 33-35, the subject matter of claim 36 would not have been obvious over Harada et al., Kanamori, and Clayton, alone or in combination.

Because the combination of Harada et al., Kanamori, and Clayton does not teach or suggest the subject matter of any of claims 33-36, and further because such combination is improper, claims 33-36 are patentable over these references. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 33-36 be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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Version With Markings to Show Changes Made

Claims 1-25 are cancelled without prejudice to their underlying subject matter.

26. (Three Times Amended) A semiconductor device, comprising:

a metallic layer over a substrate;

[an antireflective coating over said metallic layer;]

a dielectric layer over said [antireflective coating] metallic layer;

a via hole extending through the dielectric layer [and said antireflective coating] to a surface of the metallic layer;

a [preformed] titanium aluminide layer lining at least a bottom of the via hole; and

a conductive material [formed] on the titanium aluminide layer, said conductive material and said titanium aluminide layer being in contact at an interface, said interface being substantially free from tensile stress between said titanium aluminide layer and said conductive material.

27. (Three Times Amended) A semiconductor device, comprising:

an aluminum layer over a substrate;

a dielectric layer [on] over the aluminum layer;

[an antireflective coating over said dielectric layer;]

a via hole extending through the dielectric layer [and said antireflective coating] to a surface of the aluminum layer;

a [preformed] titanium aluminide layer lining at least a bottom of the via hole;

a titanium nitride layer substantially free of through cracks [formed] on the titanium aluminide layer, wherein said titanium nitride layer is in contact with said titanium aluminide layer at an interface that is substantially free of tensile stress between said titanium aluminide layer and said titanium nitride layer;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the plug material.

28. (Three Times Amended) A semiconductor memory device, comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer;

a contact interconnect between the first metallic layer and the substrate;

a second dielectric layer on the first metallic layer;

an antireflective coating over said second dielectric layer;

a via hole extending through the second dielectric layer and the antireflective coating to a surface of the second metallic layer;

a [preformed] titanium aluminide layer lining at least a bottom of the via hole [, said preformed titanium aluminide layer being volume reduced] ;

a titanium compound layer [formed] on the titanium aluminide layer and in contact with said titanium aluminide layer at an interface that is substantially free of tensile stress;

a conductive plug material on the titanium compound layer; and

a second metallic layer on the second dielectric layer and electrically connected to the plug material.

33. (Three Times Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a first metallic layer over a substrate;

a dielectric layer on the first metallic layer;

an antireflective coating over the dielectric layer;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the first metallic layer;

a [preformed] titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer [formed] on the titanium aluminide layer, said titanium compound layer being in contact with said titanium aluminide layer, wherein said titanium compound layer experiences approximately no tensile stress from said titanium aluminide layer;

a conductive plug material formed on the titanium compound layer; and

a second metallic layer on the dielectric layer and electrically connected to the plug material; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

34. (Three Times Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a metallic layer over a substrate;

a dielectric layer [on] over the metallic layer;

[an antireflective coating over said dielectric layer;]

a via hole extending through the dielectric layer [and said antireflective coating] to a surface of the metallic layer;

a [preformed] titanium aluminide layer lining at least a bottom of the via hole; and

a conductive material [formed] on the titanium aluminide layer, wherein said conductive material and said titanium aluminide layer are in contact at an interface having approximately no tensile stress from said titanium aluminide layer; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

35. (Three Times Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

an aluminum layer over a substrate;

a dielectric layer [on] over the aluminum layer;

[an antireflective coating over said dielectric layer;]

a via hole extending through the dielectric layer [and the antireflective coating] to a surface of the aluminum layer;

a [preformed] titanium aluminide layer lining at least a bottom of the via hole [, said preformed titanium aluminide layer being volume reduced] ;

a titanium nitride layer substantially free of through cracks [formed] on the titanium aluminide layer, wherein said titanium nitride layer is in contact with said titanium aluminide layer at an interface, said interface being substantially free of tensile stress between said titanium aluminide layer and said titanium nitride layer;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the plug material; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

36. (Three Times Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer;

a contact interconnect between the first metallic layer and the substrate;

a second dielectric layer [on] <u>over</u> the first metallic layer;

[an antireflective coating over the second dielectric layer;]

a via hole extending through the second dielectric layer [and the antireflective coating] to a surface of the second metallic layer;

a [preformed] titanium aluminide layer lining at least a bottom of the via hole [, said preformed titanium aluminide layer being volume reduced] ;

a titanium compound layer [formed] on the titanium aluminide layer at a contact interface, wherein said contact interface experiences approximately no tensile stress from said titanium aluminide layer;

a conductive plug material on the titanium compound layer; and

a second metallic layer on the second dielectric layer and electrically connected to the plug material; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

37. (Three Times Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a first metallic layer over a substrate;

a dielectric layer [on] over the first metallic layer;

[an antireflective coating over said dielectric layer;]

a via hole extending through the dielectric layer [and the antireflective coating] to a surface of the first metallic layer;

a [preformed] titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer [formed] on the titanium aluminide layer, wherein said titanium compound layer is in contact with said titanium aluminide layer at an

interface, said interface being substantially free of tensile stress between said titanium aluminide layer and said titanium compound layer;

a conductive plug material formed on the titanium compound layer; and

a second metallic layer on the dielectric layer and electrically connected to the plug material.

38. (Three Times Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a metallic layer over a substrate;

a dielectric layer [on] over the metallic layer;

an antireflective coating over the dielectric layer;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the metallic layer;

a preformed titanium aluminide layer lining at least a bottom of the via hole; and

a conductive material [formed] on the titanium aluminide liner, wherein said conductive material is in contact with said titanium aluminide layer at an interface, said interface being substantially free of tensile stress between said titanium aluminide layer and said conductive material.

39. (Three Times Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

an aluminum layer over a substrate;

a dielectric layer [on] over the aluminum layer;

[an antireflective coating over the dielectric layer;]

a via hole extending through the dielectric layer [and the antireflective coating] to a surface of the aluminum layer;

a [preformed] titanium aluminide layer lining at least a bottom of the via hole [, said preformed titanium aluminide layer being volume reduced];

a titanium nitride layer substantially free of through cracks [formed] on the titanium aluminide layer, wherein said titanium nitride layer is in contact with said titanium aluminide layer and said titanium aluminide layer exerts approximately zero tensile stress upon said titanium nitride layer;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the plug material.

40. (Three Times Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer;

a contact interconnect between the first metallic layer and the substrate;

a second dielectric layer [on] over the first metallic layer;

an antireflective coating over the second dielectric layer;

a via hole extending through the second dielectric layer and the antireflective coating to a surface of the second metallic layer;

a [preformed] titanium aluminide layer lining at least a bottom of the via hole [, said preformed titanium aluminide layer being volume reduced] ;

a titanium compound layer [formed] on the titanium aluminide layer, wherein said titanium compound layer is in contact with said titanium aluminide layer at an interface, said interface being substantially free of tensile stress between said titanium aluminide layer and said titanium compound layer;

a conductive plug material on the titanium compound layer; and

a second metallic layer on the second dielectric layer and electrically connected to the plug material.